In the claims:

Please cancel claims 1-9.
Please enter amended claims 10-16.

Claims 1-9 (cancelled)

10. (currently amended) A circuit for fine-tuning a voltage output comprising:

a ~~set~~ plurality of resistors ~~connected~~ coupled in parallel with each other to ~~the~~ said voltage output; ~~each resistor being connected~~

said plurality of resistors, each coupled to ground through a corresponding plurality of switching transistors; and

a ~~set~~ plurality of flip-flops ~~connected~~ correspondingly coupled to ~~the gates of~~ a gate of each of said plurality of switching transistors ~~wherein~~ a state in each of said plurality of switching transistors is configured to be ~~being~~ established by a state in [[a]] each of said plurality of ~~corresponding~~ flip-flops, where one or more said plurality of resistors ~~may be~~ are ~~connected~~ coupled to ground as determined by the states in said flip-flops.

11. (currently amended) [[A]] The circuit of claim 10, wherein ~~said data output of said flip flop~~ said plurality of flip-flops is further ~~connects~~ coupled to a default value generating means that provides a default ~~signal~~ value to the gate of each of said plurality of switching transistors ~~switch~~.

12. (currently amended) ~~A flip-flop controlled switcher~~ The circuit of claim 11, wherein said default ~~signal~~ value generating means ~~comprising~~ comprises a first default signal line and a second default signal line, said second default signal line carries a complementary signal to said first default signal line, said first and second default signal lines being ~~connected~~ coupled selectively to ~~said data outputs of said flip-flops~~ said plurality of flip-flops through a buffering means.

13. (currently amended) ~~A flip-flop controlled switcher~~ The circuit of claim 12, wherein said buffering means ~~being a~~ is at least one MOS transistor.

14. (currently amended) ~~A flip-flop controlled switches~~ The circuit of claim 10, wherein the ~~gates of a plurality of transistor switches being connected to the data outputs of a~~ plurality of flip-flops is arranged as a shift register.

15. (currently amended) A switch controlling circuit comprising:

~~N number of~~ a plurality of flip-flops, each of said plurality of flip-flops ~~of which~~ having an input terminal and an output terminal; ~~, where N is any number greater than 1,~~

said plurality of flip-flops ~~being connected~~ coupled in a serial manner to form a chain, ~~with~~ the input terminal of a first of the plurality of flip-flops serving as an input to said ~~flip-flop~~ chain of said plurality of flip-flops, ~~and~~ the output terminal of ~~the~~ a last of the plurality of flip-flops serving as an output for said ~~flip-flop~~ chain of said plurality of flip-flops; ~~, wherein~~

said input terminal of said flip-flop chain of said plurality of flip-flops ~~connects~~ being coupled to ~~an output of~~ a multiplexer output having [[a]] at least one control terminal and a plurality of input terminals, a ~~first input terminal and a second input terminal, said~~ first input terminal of said multiplexer ~~being connected~~ coupled to a data input terminal, ~~while said~~ a second input terminal ~~being connected~~ coupled to said output of said ~~flip-flop~~ chain of said plurality of flip-flops, ~~wherein~~ said plurality of flip-flops ~~are being~~ configured to be programmed by ~~shifting~~ applying data ~~in through~~ to said first input terminal of said multiplexer, ~~wherein~~ [[,]] ; and

said outputs of each of said plurality of flip-flops ~~being connected to controlling terminals of a plurality of switches, whereby signals at~~ correspondingly coupled to a plurality of switching transistors, said outputs of said plurality of flip-flops configured to activate[[s]] or deactivate[[s]] said transistor switches.

16. (currently amended) [[A]] The switch controlling circuit of claim 15, wherein the output of each of said plurality of flip-flops ~~further connects~~ further couples to a corresponding ~~drain of an~~ NMOS transistor and a corresponding ~~a~~ PMOS transistor, forming a common node that also serves as the output of ~~the~~ a transistor pair; ~~, the source of~~

a source of said PMOS transistor being coupled ~~being connected~~ to a power supply; ~~,while said source of~~

a source of said NMOS transistor being coupled ~~being connected~~ to a ground;

wherein a gate of said NMOS transistor and a gate of said PMOS transistor are each driven to pre-determined default logic values.

~~, the gate of~~

~~said NMOS transistor being connected either to a ground or a first default line while the gate of said PMOS transistor being connected either to a power supply or a second default line,~~

~~said first default line, which carries a default signal of logic 1 connects coupled to said second default line through an inverter,~~

~~wherein said gates of said PMOS and NMOS transistor pair being connected to said second default line and said ground respectively for a desired default output logic value of 1, and wherein said gates of said PMOS and NMOS transistor pair being connected said power supply and said first default line for a desired default output logic value of 0.~~